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Attorney's Docket No.: 00P7629US01/064001

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant : Schelto Van Doorn Art Unit : 2833
Serial No. : 09/574,647 Examiner : Edwin A. Leon
Filed : May 18, 2000
Title : ELECTRICALLY CONNECTING INTEGRATED CIRCUITS AND
 TRANSDUCERS

Commissioner for Patents
Wa 11-20231.

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RESPONSE

Claims 1-19 are pending. Claims 11-19 were previously withdrawn from consideration without prejudice. Claims 1-10 are rejected under 35 U.S.C. § 103(a) as being unpatentable over the applicant's admitted prior art in view of U.S. Patent No. 6,336,269 ("Eldridge"). The applicant respectfully traverses the rejections for at least the reasons stated below.

Claim 1 recites a transducer transitioning between electronic data transfer protocols of a jumper cable and an integrated circuit mounted on a substrate. The transducer includes a base mountable on the substrate, and an input/output (I/O) lead configured to directly contact an I/O lead of the integrated circuit mounted on the substrate.

The Examiner states that the applicant's admitted prior art (p. 1, lines 7-26) discloses transducers having transductional devices that can be opto-electronic devices or electronic devices, jumper cables, substrates, integrated circuits. The Examiner concedes that the applicant's admitted prior art does not show the transducer having a base mounted on the substrate, and an I/O lead configured to directly contact an I/O lead of the integrated circuit mounted on the substrate. However, the Examiner states that Eldridge discloses the concept of having an electronic component mounted in a substrate and having an I/O lead configured to directly contact an I/O lead of another electronic component mounted on the substrate. The

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Examiner further states it would have been obvious to one with ordinary skill in the art to modify the transducer of the applicant's admitted prior art by arranging the transducer and the integrated circuit board to have the I/O lead of the transducer configured to directly contact an I/O lead of the integrated circuit mounted on the substrate as shown in Eldridge in order to avoid relying on the electrical conductivity of any material on the substrate making the connection more effective.

The applicant would first like to clarify what is disclosed in the applicant's admitted prior art. The applicant disagrees with the Examiner's statement that the admitted prior art discloses "transducers having transductional devices that can be opto-electronic devices or electronic devices, jumper cables, substrates, integrated circuits." The admitted prior art discloses a transducer that produces a standardized output in accordance with prescribed protocols, regardless of the medium through which the data is transmitted or received (p. 3, lines 7-9). A transducer can transition between the transfer media of a jumper cable and the electronic data transfer protocols of the integrated circuits inside computers and peripheral devices (p. 3, lines 17-19). For example, a transducer can be an opto-electronic transceiver module providing bi-directional transmission of data (p. 3, lines 20-21). In other words, a transducer can include an opto-electronic device *transitioning between*, for example, jumper cables and integrated circuits.

The applicant respectfully disagrees with the Examiner that the admitted prior art, in view of Eldridge, discloses the transducer recited in claim 1. Specifically, the Examiner relies on the device disclosed by Eldridge in Fig 19B and at col. 91, lines 21-67 and col. 92, lines 1-26. Eldridge discloses an interposer (1900) made of a substrate (1902), such as a printed circuit board, having a plurality of holes (1904) extending therethrough, which holes are plated with a conductive material (1906) (Col. 90, lines 52-58). Eldridge uses the term "interposer" to describe a generally planar substrate having contact structures disposed on both sides thereof; contacts on one side (face) being electrically connected, within the interposer, to contacts on another side (face). Such interposers are disposed between two electronic components desired to be interconnected, and are generally used when it is not desirable to

mount contact structures directly to the electronic components being interconnected. [Col. 84, lines 55-63]

Figure 19B shows such an interposer (1900) having a first wire stem (1920) and a second wire stem (1922) bonded to the interposer (1900). In this manner, an interconnection can be made between a terminal (1942) on a first electronic component (1940) and a terminal (1952) on a second electronic component (1950). The interposer (1900) is positioned between the first and second electronic components (1940, 1950) [Col. 91, lines 1-28]. Eldridge also discloses that the first wire stem (1920) and the second wire stem (1922) can be formed as one wire stem, and thus a direct, one wire connection could be made between the terminal (1942) of the first electronic component (1940) and the terminal (1952) of the second electronic component (1950), without relying on the electrical conductivity of the through hole material (1906). However, an intermediate portion of the single wire stem (1922) would still be bonded to the terminal at the same location on the interposer (1900).

Combining the interposer disclosed by Eldridge with a transducer disclosed by the admitted prior art does not disclose each of the elements recited in the applicant's claim 1. First, Eldridge teaches an electric connection between two electronic components by way of an interposer - the interposer being a planar substrate positioned between the two electronic components. Although the electric connection may be direct in the sense that a single wire is used, the wire is still bonded to the interposer, which interposer is still used for purposes of the connection, and accordingly, Eldridge does not teach a first lead configured to directly contact a second lead, as recited in claim 1.

Second, Eldridge does not disclose the first and second electronic components as being mounted on a substrate. The Examiner states that the first electronic component (1940) and second electronic component (1950) are *mounted in a substrate*, and refers to the "substrate" as being element 1900 on Fig 19B. The applicant respectfully submits the Examiner has misconstrued Eldridge. Element 1900 in Fig 19B is the interposer itself, and the first and second element components are not mounted on or in the interposer. Rather, the interposer (1900) is positioned between the first and second electronic components. Eldridge is silent

about whether the first and second electronic components are mounted on a substrate. In fact, since a substrate (the interposer 1900) is positioned between the first and second electronic components, it would seem unlikely the first and second electronic components could be mounted on a single substrate, and accordingly, Eldridge seems to teach away from mounting the first and second electronic components on a substrate.

Third, the Examiner has failed to provide a motivation to combine the interposer disclosed by Eldridge and the transducer disclosed in the admitted prior art. Eldridge's interposer is used when it is "not desirable to mount contact structures directly to the electronic components being interconnected" (Col. 84, lines 60-63). By contrast, claim 1 recites a transducer having an I/O lead configured to directly contact an I/O lead of an integrated circuit. There is no need to use an interposer, as the transducer includes an I/O lead. Accordingly, there is no motivation to combine the interposer of Eldridge with a transducer having an I/O lead.

Further, Eldridge actually teaches away from the limitation recited in claim 1, since the transducer and integrated circuit recited in claim 1 each include a lead, which is contrary to Eldridge's teaching of using an interposer rather than mounting a contact structure, such as a lead, directly to an electronic component.

The applicant's admitted prior art, in view of Eldridge, clearly fails to teach each and every element recited in claim 1, and a *prima facie* case of obviousness has not been established. Claim 1 is therefore in condition for allowance. Claims 2-10 depend from claim 1, and are therefore allowable for at least the same reasons.

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Applicant asks that all claims be allowed. No fees are believed due, however please apply any charges or credits to Deposit Account No. 06-1050.

Respectfully submitted,

Date: Jan 22/03

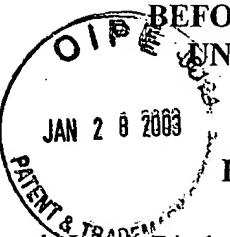


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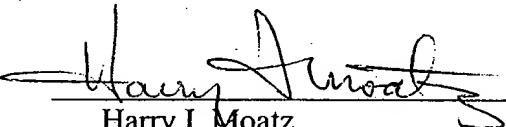
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